COMPLETE LISTING OF CLAIMS

1 – 21 (Canceled)

22 - 30 (Withdrawn)

31 – 48 (Canceled)

49. (Previously added) A semiconductor wafer including an integrated chip scale package to be used for integrated circuits, the wafer comprising:

a top surface and a bottom surface; and

wherein the semiconductor wafer is an unprocessed wafer having no active circuit layers or interconnect layers present on said top surface or said bottom surface of the semiconductor wafer;

a plurality of vias formed in the unprocessed semiconductor wafer, each via having a via top portion beginning at said top surface of the unprocessed semiconductor wafer and extending through to a via bottom portion on said bottom surface of the unprocessed semiconductor wafer;

wherein at least some of said plurality of vias include an input/output (I/O) interconnect structure physically and electrically coupled to said via bottom portion, and said I/O interconnect structure is located within an area on the bottom surface of the unprocessed wafer; and

wherein the I/O interconnect structure is adapted such that an active circuit which is fabricated on the unprocessed semiconductor wafer as part of an integrated circuit at a later time than the I/O interconnect structure can be electrically connected to another integrated circuit without requiring further packaging operations to form pads or bumps for connecting I/O signals of such active circuit to such another integrated circuit.

50. (Previously added) The semiconductor wafer of claim 49, wherein at least some of said plurality of vias are filled with a conductive material capable of withstanding a high temperature cycle associated with a manufacturing operation used later to make said active circuit.

51. (Previously added) The semiconductor wafer of claim 49, wherein at least some of said plurality of vias are filled with an insulating material capable of providing support for the semiconductor wafer during a manufacturing operation used later to make said active circuit.

52. (Previously added) The semiconductor wafer of claim 49 wherein said via is substantially larger than a minimum feature size used in fabricating said active circuit.

53. (Previously added) The semiconductor wafer of claim 52, wherein said via is about 4 mils in diameter.

54. (Previously added) The semiconductor wafer of claim 49, further including a passivation layer formed on at least said top surface.

55. (Previously added) The semiconductor wafer of claim 49, wherein the input/output (I/O) interconnect structure includes a plurality of solder bumps and/or pads.

56. (Previously added) The semiconductor wafer of claim 49, wherein the semiconductor wafer includes a plurality of chip-scale packages.

57. (Previously added) The semiconductor wafer of claim 55, further including a plurality of integrated circuits on the semiconductor wafer coupled to said plurality of chip-scale packages.

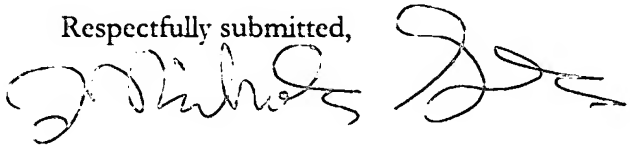
58. (Previously added) The semiconductor wafer of claim 55, wherein said plurality of integrated circuits on the semiconductor wafer are memory devices.

59. (Previously added) The semiconductor wafer of claim 55, further including a second I/O structure on a top surface of the semiconductor wafer.

60. (Previously added) The semiconductor wafer of claim 55, wherein said bottom portion for at least some of said plurality of vias is substantially larger than a corresponding top portion.

No fees are believed to be due since the supplemental response was adequate within the requirements of the restriction requirement made by the Examiner. If any fees are due, please charge any fees to deposit account no. 233 - 264.

Respectfully submitted,



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I hereby certify that the foregoing is being deposited with the U.S. Postal Service to Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, this 17th day of February 2005.